REMARKS

Claims 1-9 are pending in this application; claim 1 being independent. In light of the remarks made herein, Applicants respectfully request reconsideration and withdrawal of the outstanding rejections.

The Official Action

In the outstanding Official Action, the Examiner objected to the drawings under 37 C.F.R. § 1.83(a); rejected claims 1-9 under 35 U.S.C. § 112, second paragraph; and rejected claims 1-3 and 7 under 35 U.S.C. § 102(b) as being anticipated by *Muramatsu et al.* (USP 5,373,204). Applicants respectfully traverse these rejections.

Allowable Subject Matter

Applicants wish to thank the Examiner for noting the allowability of claims 4-6, 8, and 9 if rewritten to overcome the rejections under 35 U.S.C. § 112, second paragraph.

Objection to the Drawings

The Examiner objected to the drawings under 37 C.F.R. § 1.83(a), asserting the drawings must show every feature of the invention specified in the claims. Specifically, the Examiner asserted "said first storage means being reset by an input of said fourth pulse" and "said second storage means storing said fourth pulse" as cited in claims 4, 8, and 9 were not shown.

The Examiner's attention is respectfully directed to Fig. 2 and its related discussion in the specification depicting an exemplary first storage means being reset by an input of the fourth pulse and an exemplary second storage means storing the fourth pulse as cited in claims 4, 8, and 9. For example, the first storage means may be realized by RS flipflop 111,

the second storage means may be realized by RS flipflop 112, and the first and second storage means receiving the fourth pulse may be realized by output G from the logic means NAND gate 141. As such, it is respectfully submitted that these elements of the claims are exemplarily depicted in Fig. 2 and, thus, it is respectfully requested that the outstanding objection to the drawings be withdrawn.

Claim Rejections - 35 U.S.C. § 112

With regard to the Examiner's rejection of claim 1 under 35 U.S.C. § 112, second paragraph, by this Amendment, Applicants have amended claim 1 to more appropriately recite the present invention. Based upon the amendments made herein, Applicants respectfully request withdrawal of the outstanding rejection.

Claim Rejections - 35 U.S.C. § 102

With regard to the Examiner's rejection of claim 1 under 35 U.S.C. § 102(b) as being anticipated by *Muramatsu et al.*, the Examiner asserts that *Muramatsu et al.* teaches the adjustment unit of the present invention, citing to Fig. 1, reference 14.

It is respectfully submitted that *Muramatsu et al.* teaches a self-timed clocking transfer control circuit. Specifically, *Muramatsu et al.* teaches

> Transfer control circuit 14 includes a transfer request signal input terminal (CI input terminal) 40 for receiving a transfer request signal CI (C10) from a preceding stage (not shown), a transfer acknowledge output terminal (RO output terminal) 42 for outputting a transfer acknowledge signal RO (R10) indicating to the preceding stage acknowledgement or prohibition of transfer, a transfer request signal output terminal (CO output terminal) 44 for outputting a transfer request signal CO (C10) to a succeeding stage (not shown), a transfer acknowledge input terminal (RI input terminal) 46 for receiving from the succeeding stage a transfer acknowledge signal RI (R20) indicating acknowledgement or prohibition of transfer, and an output terminal for

> providing data holding circuit 12 (shown in FIG. 2) with a clock pulse CP for controlling data holding operation. (Col. 1, line 62 - col. 2, line 9).

In contrast, the present invention as set forth in claim 1, as amended, recites, *inter alia*, a data transmission line comprising an adjustment unit for adjusting timing of input of the data output from the synchronous system and the data transmitted in the asynchronous system from the preceding stage to the data holding unit by the transfer control unit when a mode in which data output from the synchronous system is taken and transmitted to the data transmission line.

It is respectfully submitted that *Muramatsu et al.* fails to teach the adjustment unit of the present invention. As noted above, *Muramatsu et al.* teaches transfer control unit 14 provides data holding circuit 12 (additionally depicted in Fig. 2) with a clock pulse CP for controlling data holding operation. It is respectfully submitted that *Muramatsu et al.* fails to teach an adjustment unit for adjusting timing of input of the data output from the synchronous system and the data transmitted in the asynchronous system from the preceding stage to the data holding unit, by the transfer control unit, when a mode in which data output from the synchronous system is taken and transmitted to the data transmission line. As such, it is respectfully submitted that claim 1, together with claims dependent thereon, are not anticipated by *Muramatsu et al.*

CONCLUSION

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Catherine M. Voisinet (Reg. No. 52,327) at (703) 205-8000, to conduct an interview in an effort to expedite prosecution in connection with the present application.

Applicants respectfully petition for a one (1) month extension of time pursuant to 37 C.F.R. §§ 1.17 and 1.136(a). A check in the amount of $110.00 in payment of the extension of time fee is attached.

If necessary, the Commissioner is hereby authorized in this, concurrent, and further replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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By _____
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CG/CMV/jdm
0033-0599P

Attachment: Version With Markings to Show Changes Made

(Rev. 02/12/01)

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

1. (Amended) A data transmission line used continuously connected [continuously] in a plurality of stages in an asynchronous system, comprising:

a data holding unit receiving and holding data transmitted from a preceding stage or data output from an external synchronous system, and outputting and transmitting the data to a succeeding stage;

a transfer control unit for controlling input and output of said data at said data holding unit; and

an adjustment unit for adjusting timing of input of the data output from said synchronous system and the data transmitted in the asynchronous system from said preceding stage to said data holding unit, by said transfer control unit, when a mode in which data output from said synchronous system is taken and transmitted to said data transmission line [, is designated timing of input of the data output from said synchronous system and the data transmitted in the asynchronous system from said preceding stage to said data holding unit, by said transfer control unit].